ABSTRACT

The semiconductor memory device has a memory capacity that can be increased without increasing the load to bit lines and has increased access speed. Because the output lines of bit line selector circuits 20 through 27 are precharged by charge circuits 30 through 37, and selectable bit lines (SBL, SBLZ) reach a high level before access is gained for reading from memory cells, data read previously is held unchanged for output signal SAOUT of data latch circuit 70. Because output lines of bit line selector circuits 20 through 27 are all at the high level even when another gate circuit becomes conductive as a new read address is set, the selected bit lines remains at the high level, and data previously read is held unchanged for output signal SAOUT of data latch circuit 70. Output signal SAOUT of data latch circuit 70 is changed to the next data read as soon as differential amplification operation of the bit lines is completed by amplifier circuits 40 through 47.